PROCESSOR HAVING SELECTIVE BRANCH PREDICTION

Abstract of the Disclosure

A data system capable of selecting whether to utilize address prediction based on the state of an address prediction enable signal. When employing address prediction, the outcome of branch instructions are presumed prior to the resolution of the instruction. When not using address prediction, the system waits until a branch instruction is resolved before fetching the next address to be executed. At least one embodiment of a method and data system disclosed herein makes use of the different setup timing available when employing prediction and non-prediction modes of operation.